

5 WHAT IS CLAIMED IS:

1. An interconnect for a semiconductor component having a component contact comprising:

a substrate; and

10 a compliant conductive layer on the substrate comprising a tip portion for contacting the component contact, a shaped spring segment portion supporting the tip portion, and a hollow interior portion at least partially enclosed by the spring segment portion and the tip portion.

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2. The interconnect of claim 1 wherein the shaped spring segment portion has a stepped shape open on two sides.

20 3. The interconnect of claim 1 wherein the shaped spring segment portion has a dome shape or a conical shape substantially enclosing the hollow interior portion.

25 4. The interconnect of claim 1 wherein the compliant conductive layer comprises a metal, a conductive polymer or a tape material.

30 5. The interconnect of claim 1 wherein the compliant conductive layer comprises a conductive polymer comprising a plurality of metal particles configured to penetrate the component contact.

35 6. The interconnect of claim 1 wherein the tip portion includes a penetrating structure comprising an element selected from the group consisting of points, blades and particles.

5 7. The interconnect of claim 1 wherein the compliant
conductive layer includes a base portion comprises a metal
deposited in an opening in the substrate.

8. The interconnect of claim 1 wherein the compliant
10 conductive layer includes a base portion on the substrate
and the shaped spring segment portion has a generally
conical shape.

9. The interconnect of claim 1 further comprising a
15 plurality of compliant conductive layers corresponding to a
plurality of component contacts on the component.

10. The interconnect of claim 1 wherein the component
is contained on a semiconductor wafer comprising a
20 plurality of components.

11. The interconnect of claim 1 wherein the component
comprises a semiconductor package and the component
contacts comprise bumps.

25 12. The interconnect of claim 1 wherein the component
contacts comprise planar pads.

13. The interconnect of claim 1 wherein the component
30 comprises a semiconductor die or a semiconductor package
contained on a wafer.

14. An interconnect for a semiconductor component
having a component contact comprising:

35 a substrate; and
a compliant conductive layer on the substrate having a
stepped shape and a hollow interior portion, the layer
having a base portion on the substrate, a tip portion for

5 contacting the component contact, and a spring segment
portion configured to allow flexure of the tip portion.

15. The interconnect of claim 14 wherein the
substrate comprises a material selected from the group
10 consisting of a semiconductor material, a plastic material
and a ceramic.

16. The interconnect of claim 14 wherein the
compliant conductive layer includes a penetrating structure
15 for penetrating the component contact.

17. The interconnect of claim 14 wherein the
compliant conductive layer comprises a polymer tape having
a polymer substrate and a conductive layer on the polymer
20 substrate.

18. The interconnect of claim 14 wherein the
compliant conductive layer comprises a conductive polymer
comprising a plurality of particles configured to penetrate
25 the component contact.

19. The interconnect of claim 14 further comprising a
conductor on the substrate in electrical communication with
the compliant conductive layer.
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20. The interconnect of claim 14 further comprising a
conductive via in the substrate in electrical communication
with the compliant conductive layer.

35 21. The interconnect of claim 14 further comprising a
plurality of compliant conductive layers on the substrate
corresponding to a plurality of component contacts on the
component.

5 22. The interconnect of claim 14 wherein the
component is contained on a semiconductor wafer.

 23. An interconnect for a semiconductor component
having a plurality of component contacts comprising:

10 a substrate; and

 a plurality of interconnect contacts on the substrate
configured to electrically engage the component contacts,
each interconnect contact comprising a base portion on the
substrate, a shaped spring segment portion on the base
15 portion, and a tip portion on the spring segment portion
for contacting a component contact.

 24. The interconnect of claim 23 wherein the
component is contained on a semiconductor wafer containing
20 a plurality of components and the interconnect contacts are
configured to electrically engage all of the component
contacts on the wafer.

 25. The interconnect of claim 23 wherein the base
25 portion is contained in an opening in the substrate.

 26. The interconnect of claim 23 wherein the shaped
spring segment portion has a stepped shape.

30 27. The interconnect of claim 23 wherein the shaped
spring segment portion has a generally square shape.

 28. The interconnect of claim 23 wherein the shaped
spring segment portion has a dome shape.

35 29. An interconnect for a semiconductor component
having a plurality of component contacts comprising:

 a substrate; and

5 a plurality of interconnect contacts on the substrate
configured to electrically engage the component contacts,
each component contact comprising a compliant conductive
layer having a dome shape and a hollow, substantially
enclosed, interior portion, the layer having a base portion
10 on the substrate and a tip portion for contacting a
component contact.

30. The interconnect of claim 29 wherein the
component is contained on a semiconductor wafer containing
15 a plurality of components and the interconnect contacts are
configured to electrically engage all of the component
contacts on the wafer.

31. The interconnect of claim 29 wherein the
20 compliant conductive layer includes an opening to the
interior portion.

32. The interconnect of claim 29 wherein the
compliant conductive layer comprises a metal.

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33. The interconnect of claim 29 wherein the
compliant conductive layer comprises a polymer tape having
a polymer substrate and a conductive layer on the polymer
substrate.

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34. The interconnect of claim 29 wherein the
compliant conductive layer comprises a conductive polymer
comprising a plurality of particles configured to penetrate
the component contact.

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35. The interconnect of claim 29 wherein the tip
portion has an enclosed spring shape.

5 36. An interconnect for a semiconductor component having a component contact comprising:

 a substrate having an opening; and

 a compliant conductive layer on the substrate comprising a base portion lining the opening, a shaped
10 spring segment portion attached to base portion, and a tip portion on the shaped spring segment portion configured to contact the component contact.

 37. The interconnect of claim 36 further comprising a
15 stop plane element on the substrate configured to limit axial movement of the tip portion.

 38. The interconnect of claim 36 wherein the spring segment portion has a generally conical shape.

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 39. The interconnect of claim 36 wherein the tip portion has an enclosed spring shape.

 40. The interconnect of claim 36 wherein the
25 substrate comprises a material selected from the group consisting of a semiconductor, a plastic and a ceramic.

 41. The interconnect of claim 36 wherein the compliant conductive layer comprises a metal selected from
30 the group consisting of Ti, Cu, Al, W, Mo, Ta, Be, Mg and alloys of these metals.

 42. An interconnect for a semiconductor component having a plurality of component contacts comprising:

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 a substrate; and

 a plurality of interconnect contacts on the substrate configured to electrically engage the component contacts, each interconnect contact comprising an opening in the substrate, a base portion lining the opening, a spring

5 segment portion attached to base portion having an enclosed interior portion, and a tip portion on the spring segment portion configured to move in an axial direction to contact the component contact.

10 43. The interconnect of claim 42 wherein the spring segment portion is generally conically shaped.

44. The interconnect of claim 42 further comprising a polymer layer configured to limit movement of the tip
15 portion during contact with the component contact.

45. The interconnect of claim 42 further comprising a polymer donut circumjacent to the opening configured to limit movement of the tip portion during contact with the
20 component contact.

46. The interconnect of claim 42 further comprising a conductor on the substrate in electrical communication with the base portion and a terminal contact on the substrate in
25 electrical communication with the conductor.

47. The interconnect of claim 42 wherein the component comprises a semiconductor package and the component contacts comprise bumps.
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48. The interconnect of claim 42 wherein the component contacts comprise planar pads.

49. The interconnect of claim 42 wherein the
35 component comprises a semiconductor die or a semiconductor package contained on a wafer.

50. The interconnect of claim 42 wherein the substrate comprises silicon.

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51. A method for fabricating an interconnect for a semiconductor component having a component contact comprising:

providing a substrate;

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shaping the substrate;

forming a conductive layer on a shaped portion of the substrate; and

removing the shaped portion to form a compliant conductive layer configured to electrically contact the component contact.

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52. The method of claim 51 wherein the shaping step comprises etching the substrate.

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53. The method of claim 51 wherein the shaped portion has a stepped shape or a dome shape.

54. The method of claim 51 further comprising forming a conductor on the substrate in electrical communication with the compliant conductive layer.

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55. The method of claim 51 wherein the compliant conductive layer comprises a base portion on the substrate, a tip portion configured to contact the component contact, and a spring segment portion configured to support the tip portion for movement in an axial direction.

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56. The method of claim 51 wherein the substrate comprises a material selected from the group consisting of a semiconductor, a plastic and a ceramic.

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5 57. The method of claim 51 wherein the compliant
conductive layer comprises a metal selected from the group
consisting of Ti, Cu, Al, W, Mo, Ta, Be, Mg and alloys of
these metals.

10 58. A method for fabricating an interconnect for a
semiconductor component having a component contact
comprising:

 providing a substrate;

 shaping the substrate to form a shaped portion
15 thereof;

 forming a conductive layer on the shaped portion and
on the substrate having an opening configured to permit
access to the shaped portion; and

 etching through the opening to remove the shaped
20 portion and form a compliant conductive layer configured to
electrically engage the component contact.

 59. The method of claim 58 wherein the opening
comprises an open end of the conductive layer.

25 60. The method of claim 58 wherein the conductive
layer substantially encloses the shaped portion.

 61. The method of claim 58 wherein the shaped portion
30 has a stepped shape or a dome shape.

 62. The method of claim 58 wherein the shaping step
comprises forming a mask on the substrate and etching the
substrate.

5 63. The method of claim 58 wherein the substrate
comprises a material selected from the group consisting of
a semiconductor, a plastic and a ceramic.

10 64. The method of claim 58 wherein the conductive
layer comprises a conductive polymer containing a plurality
of particles configured to penetrate the component contact.

15 65. The method of claim 58 further comprising forming
a penetrating structure on the compliant conductive layer
configured to penetrate the component contact.

20 66. A method for fabricating a semiconductor
component having a component contact comprising:
 providing a substrate;
 forming a shaped opening in the substrate;
 depositing a conductive material in the shaped
opening; and
 removing a portion of the substrate proximate to the
shaped opening to form a compliant conductive layer
25 configured to electrically engage the component contact.

30 67. The method of claim 66 wherein the forming the
shaped opening step comprises laser machining or etching
the substrate.

35 68. The method of claim 66 wherein the shaped opening
has a cylindrical portion, a counterbored portion, and a
tip opening and the compliant conductive layer comprises a
base portion on the cylindrical portion, a spring segment
portion formed by the counterbored portion and a tip
portion formed by the tip opening.

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69. The method of claim 66 further comprising forming a conductor on the substrate in electrical communication with the compliant conductive layer.

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70. The method of claim 66 wherein the removing step comprises etching the substrate.

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71. The method of claim 66 further comprising forming a polymer layer on the substrate having an opening circumjacent to the complaint conductive layer configured to limit axial movement thereof during electrical engagement of the component contact.

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72. A method for fabricating a semiconductor component having a component contact comprising:

providing a substrate;

forming an opening in the substrate having a selected shape;

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depositing a conductive material in the opening having a tip portion and a spring segment portion; and

removing the substrate and a portion of the shaped opening to expose the tip portion and the spring segment portion to form an interconnect contact configured to electrically engage the component contact.

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73. The method of claim 72 wherein the forming the shaped step comprises laser machining or etching the substrate.

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74. The method of claim 72 wherein the removing the substrate step comprises etching the substrate.

5 75. The method of claim 72 wherein the removing the substrate step comprises thinning the substrate.

76. The method of claim 72 wherein the interconnect contact comprises a base portion comprising the conductive
10 material in the opening following the removing step.

77. The method of claim 72 wherein the spring segment portion has a generally conical shape and an enclosed interior portion.

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78. The method of claim 72 wherein the substrate comprises a material selected from the group consisting of a semiconductor, a plastic and a ceramic.

20 79. The method of claim 72 further comprising forming a conductor on the substrate in electrical communication with the conductive material.

80. The method of claim 72 further comprising forming
25 a polymer donut on the substrate circumjacent to the tip portion configured to limit axial movement of the tip portion.

81. A system for testing a semiconductor wafer
30 containing a plurality of semiconductor components having a plurality of component contacts comprising:

 a test circuitry configured to apply test signals to the components;

 a testing apparatus configured to support and move the
35 wafer;

 an interconnect on the testing apparatus comprising a substrate and a plurality of interconnect contacts on the substrate in electrical communication with the test

5 circuitry and configured to electrically engage the
component contacts,

10 each interconnect contact comprising a compliant
conductive layer on the substrate comprising a tip portion
for contacting a component contact, a shaped spring segment
portion supporting the tip portion, and a hollow interior
portion at least partially enclosed by the spring segment
portion and the tip portion.

15 82. The system of claim 81 wherein the testing
apparatus comprises a wafer probe handler.

20 83. The system of claim 81 further comprising a
plurality of spring loaded electrical connectors on the
testing apparatus configured to electrically engage
terminal contacts on the substrate in electrical
communication with the interconnect contacts.

25 84. The system of claim 81 wherein the interconnect
contacts comprise penetrating structures configured to
penetrate the component contacts.

 85. The system of claim 81 wherein the compliant
conductive layer comprises a metal or a conductive polymer.

30 86. A system for testing a semiconductor wafer
containing a plurality of semiconductor components having a
plurality of component contacts comprising:

 a test circuitry configured to apply test signals to
the components;

35 a wafer probe handler configured to support and move
the wafer; and

 an interconnect on the wafer probe handler comprising
a substrate, and a plurality of interconnect contacts on
the substrate configured to electrically engage the

5 component contacts, each interconnect contact comprising a base portion on the substrate, a shaped spring segment portion on the base portion, and a tip portion on the spring segment portion for contacting a component contact.

10 87. The system of claim 86 wherein the wafer probe handler includes a probe card fixture and the interconnect mounts to the probe card fixture.

15 88. A system for testing a semiconductor wafer containing a plurality of semiconductor components having a plurality of component contacts comprising:

a test circuitry configured to apply test signals to the components;

20 a wafer probe handler configured to support and move the wafer; and

an interconnect on the wafer probe handler comprising a substrate, and a plurality of interconnect contacts on the substrate configured to electrically engage the component contacts, each interconnect contact comprising
25 a compliant conductive layer comprising a base portion lining an opening in the substrate, a shaped spring segment portion attached to base portion, and a tip portion on the shaped spring segment portion configured to contact a component contact.

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89. The system of claim 88 further comprising a stop plane element on the substrate configured to limit axial movement of the tip portion.

35 90. The system of claim 88 wherein the spring segment portion has a generally conical shape.

91. The system of claim 88 wherein the tip portion has an enclosed spring shape.

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92. A system for testing a semiconductor component having a plurality of component contacts comprising:

a test circuitry configured to apply test signals to the components;

10 a test carrier configured to retain the component; and
an interconnect on the test carrier comprising a substrate and a plurality of interconnect contacts on the substrate in electrical communication with the test circuitry and configured to electrically engage the
15 component contacts,

each interconnect contact comprising a base portion on the substrate, a shaped spring segment portion on the base portion, and a tip portion on the spring segment portion for contacting a component contact.

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93. The system of claim 92 wherein the test carrier comprises a force applying mechanism configured to bias the component against the interconnect.

25 94. The system of claim 92 wherein each interconnect contact comprises a penetrating structure configured to penetrate the component contact.

30 95. A system for testing a semiconductor component having a component contact comprising:

a test circuitry configured to apply test signals to the component;

a test apparatus configured to handle the component; and

35 an interconnect on the test apparatus comprising a substrate, and a plurality of interconnect contacts on the substrate in electrical communication with the test circuitry and configured to electrically engage the component contacts,

5 each interconnect contact comprising an opening in the
substrate, a base portion lining the opening, a spring
segment portion attached to base portion having an enclosed
interior portion, and a tip portion on the spring segment
portion configured to move in an axial direction to contact
10 the component contact.

96. The system of claim 95 further comprising a
polymer layer configured to limit movement of the tip
portion during contact with the component contact.

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97. The system of claim 95 further comprising a
polymer donut circumjacent to the opening configured to
limit movement of the tip portion during contact with the
component contact.

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98. The system of claim 95 wherein the component
comprises a semiconductor wafer and the test apparatus
comprise a wafer probe handler.

25 99. The system of claim 95 wherein the component
comprises a semiconductor die or a semiconductor package
and the test apparatus comprises a test carrier.

30 100. The system of claim 95 wherein the 87 test
apparatus comprises a wafer probe handler with a probe card
fixture and the interconnect mounts to the probe card
fixture.

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